AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A semiconductor chip with a rectangular main surface and a functional element comprising:

a first side composing said main surface;

a second side composing said main surface, wherein the second side is opposite to said first side;

a main electrode pad group composed of a plurality of main electrode pads, wherein said plurality of main electrode pads is arranged on said main surface along said first side;

a first electrode pad group composed of a plurality of first electrode pads, which is located between said first side and said main electrode pad group with a first distance, wherein said plurality of first electrode pads is arranged on said main surface along said first side;

a second electrode pad group composed of a plurality of second electrode pads, which is located between said second side and said main electrode group with a second distance that is longer than said first distance, wherein said plurality of second electrode pads is arranged on said main surface along said second side;

a plurality of first interconnections, wherein each first interconnection is connected between one of the main electrode pads and one of the first electrode pads; and

a plurality of second interconnections, wherein each second interconnection is connected between one of the main electrode pads and one of the second electrode pads,

wherein a main electrode pad connecting to a first electrode pad and a main electrode pad connecting to a second electrode pad are arranged alternately.

2. (Previously Presented) The semiconductor chip according to claim 1,

wherein said first interconnections and said second interconnections are provided on said main surface of said semiconductor chip.

3. (Previously Presented) The semiconductor chip according to claim 1,

wherein said first interconnections and said second interconnections are provided within said semiconductor chip.

4. (Previously Presented) The semiconductor chip according to claim 3, wherein any one or both of said first interconnections and said second interconnections have a multi-layer wired structure.

Claims 5-12 (Canceled)

13. (Previously Presented) The semiconductor chip according to claim 1, wherein any one or both of said first and second interconnections are formed within a same wired layer.

14. (Previously Presented) The semiconductor chip according claim 1, wherein said semiconductor chip is provided with a multi-layer wired structure; and any one or both of said first and second interconnections has or have the multi-layer wired structure, which comprises a plurality of wired layers connected through a via embedded in a via hole.

15. (Previously Presented) The semiconductor chip according to claim 1, wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of a lower side of said main electrode pad group.

16. (Previously Presented) A semiconductor device comprising:

a substrate having a first front surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range;

a first semiconductor chip having a rectangular main surface and a functional element laminated in said third range of said first front surface; said first semiconductor chip having a first side composing said main surface; a second side composing said main surface, wherein the second side is opposite to said first side; a main electrode pad group composed of a

plurality of main electrode pads, wherein said plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group composed of a plurality of first electrode pads which is located between said first side and said main electrode pad group with a first distance, wherein said plurality of first electrode pads is arranged on said main surface along said first side; a second electrode pad group composed of a plurality of second electrode pads which is located between said second side and said main electrode group with a second distance which is longer than said first distance, wherein plurality of second electrode pads is arranged on said main surface along said second side; a plurality of first interconnections, wherein each first interconnection is connected between one of the main electrode pads and one of the first electrode pads; and a plurality of second interconnections, wherein each second interconnection is connected between one of the main electrode pads and one of the second electrode pads;

a second semiconductor chip having the same configuration of the first semiconductor chip and mounted on said first semiconductor chip laminated in said main surface;

a first bonding wire electrically connecting between said first bonding pad and said first electrode pad of said first semiconductor;

a second bonding wire electrically connecting between said main electrode pad of said first semiconductor chip and a first electrode pad of said second semiconductor chip, wherein said main electrode pad of said first semiconductor chip is connected with said first electrode pad of said first semiconductor chip through said first interconnection of said first semiconductor chip;

a third bonding wire electrically connecting between said main electrode pad of said first semiconductor chip and a main electrode pad of said second semiconductor chip, wherein said main electrode pad of said first semiconductor chip is connected with said second electrode pad of said first semiconductor chip through said second interconnection of said first semiconductor chip, and said main electrode pad of said second semiconductor chip is connected with a second electrode pad of said second semiconductor chip through a second interconnection of said second semiconductor chip; and

a fourth bonding wire electrically connecting between said second bonding pad and said second electrode pad of said second semiconductor chip;

wherein, in said first semiconductor chip and said second semiconductor chip, said

first side of said first semiconductor chip and a first side of said second semiconductor chip are located at the same side, said main surface of said first semiconductor ship and a main surface of said second semiconductor chip are turned in the same direction, and said main electrode pad and said first electrode pad of said first semiconductor chip are located at the outside from a first side of said second semiconductor chip.

Claims 17-25 (Canceled)

26. (Previously Presented) The semiconductor chip according to claim 16, wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of a lower side of said main electrode pad group.

27. (Previously Presented) The semiconductor chip according to claim 16, wherein said substrate is provided with a via hole passing through from said first front surface to a second surface of the substrate, a via embedded in the via hole and connected to one of said plurality of first and second bonding pads, and an external terminal connected to said via; and said substrate is further provided with a sealing portion sealing all bonding wires on said substrate.